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17 FEBRUARY 1999 (17. 02. 99) International Filing Date
INTERNATIONAL BUREAU OF WIPO PCT International Application Name of receiving Office and "PCT International Application"

Applicant's or agent's file reference *(if desired) (12 characters maximum)* SZ9-98-049

Box No. I TITLE OF INVENTION

CONTROLLED SWITCHING EFFECT IN DEVICES WITH SLIGHTLY DOPED OXIDE INSULATOR

Box No. II APPLICANT

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)*

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request	: 4
description (excluding sequence listing part)	: 19
claims	: 7
abstract	: 1
drawings	: 4
sequence listing part of description	:
Total number of sheets	: 35

This international application is **accompanied by** the item(s) marked below:

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Controlled Switching Effect in Devices with Slightly Doped Oxide Insulator

1. BACKGROUND OF THE INVENTION

1.1 FIELD OF THE INVENTION

The present invention relates to electronic and microelectronic devices. In particular, the present invention relates to a plurality of materials showing a switching phenomenon and a built-in memory by the aid of which a new principle of storing and reading information in memory cells of semiconductor chips and a plurality of fundamental improvements on electronic or microelectronic devices can be achieved.

1.2 DESCRIPTION AND DISADVANTAGES OF PRIOR ART

Although the present invention is applicable in a broad variety of microelectronic or electronic applications it will be described with the focus put on an application to memory cells as RAM, for example.

The need to remain cost and performance competitive in the production of semiconductor devices has caused continually increasing device density in integrated circuits. To facilitate the increase in device density, new technologies are constantly needed to allow the feature size of these semiconductor devices to be reduced.

Conventional DRAM cells consist of a transistor and a capacitor mostly made from Silicon dioxide SiO2 . They need the transistor to control the inflow and outflow of charge stored in the capacitor as the physical quantity exploitable for storing information. Said transistor also decouples the capacitors from

each other. Such DRAM cells have the disadvantage, that information stored therein is volatile and as such can principally be lost on each power supply failure. Further, the time needed to refresh the information contained in DRAM cells delimits the read and write performance of such cells. Finally the structure of such a DRAM cell is quite complex due to the required transistor.

Thus, a change in computer RAM technology beyond conventional DRAM technology would be desirable.

The use of ferroelectric nonvolatile RAM (NVRAM) cells would already be a great step forward as information would not be lost on any power failure although the structure of the memory cell would remain complex, too. In such ferroelectric RAMs the polarization of the bit storing layer is exploited instead of a capacitor's capacity in DRAM cells for defining two different states which can be associated with two different logical values. A long term switching between different polarization states, however, fatigues the ferroelectric properties of the material, as e.g. lead zirconium titanate (PZT). Further, the retooling costs for the chip industry would be enormous. Thus, such materials do not meet the actual requirements for RAM elements, until now.

In 'Physics Today' July 1998, page 24 a further high permittivity material and a respective semiconductor fabricating technology is proposed which allows the computer industry to use the equipment of its conventional DRAM manufacturing plants without to perform basic retooling. It is the so-called high permittivity DRAM technology.

Herein, the charge of a capacitor can be used to store information as it is done in conventional DRAM technology as the

polarization of a high permittivity layer depends linearly on the applied voltage, as required for charging the DRAM capacitors. A high permittivity material as e.g. barium strontium titanate (BST) having a permittivity „r about 500 instead of „r about 4 for silicon dioxide would allow to reduce the space needed for the capacitor as its capacitance is proportional to its area and the magnitude of its permittivity value. This in turn would allow higher integration levels compared to conventional silicon oxide materials used in DRAM cells as the capacitor's area consumption is large as compared to that of the coupled transistor.

But, nevertheless, as a disadvantage remains that the leakage current is still large. Thus, refreshing is a must.

Finally, with increasing integration near and beyond the 1 Gbit chip due to smaller capacitor size the area consumption of the transistor of a memory cell is not neglegible anymore. Thus, a great step forward to ULSI would be to get the structure of a memory cell as simple as possible.

<u>1.3 OBJECTS OF THE INVENTION</u>

Therefore, an object of the present invention is to provide a robust simply structured and nonvolatile memory cell.

It is another object of the present invention to provide a new simpler method for stable storage of information into such a memory cell and a reproducible erasing and reading from it.

It is another object of the present invention to provide a simply structured and nonvolatile memory cell which is able to

store more then only two distinct values, i.e., which is ready for multilevel storage.

2. SUMMARY AND ADVANTAGES OF THE INVENTION

These objects of the invention are achieved by the features stated in enclosed independent claims. Further advantageous arrangements and embodiments of the invention are set forth in the respective subclaims.

The basic discovery underlying the present invention concerns a plurality of oxide substances including perovskites and related compounds, i.e materials, for use in microelectronic and in electronic circuits and particularly for use in semiconductor chips which combines both, a switching phenomenon in resistance and a built-in memory.

In general and coinciding with the wording of the appended claims substances are claimed comprising components A_x, B_y, and oxygen O_z, in which substance

said component A is a member of Alkaline metals (group IA), or Alkaline Earth metals (group IIA), or Rare Earth elements, or Scandium, or Yttrium,
said component B is a transition metal being member of one of the groups IB to VIII, or a member of one of the groups IIIA, IVA, VA and the substance has a crystalline structure.

Generally, an elementary cell of the corresponding lattice structure comprises a cell center molecule which is surrounded by a plurality of oxygene molecules each having in turn a center molecule. Both types of said center locations can principally be taken by either of the component A, or B, respectively. In other words, there are a plurality of substances, i.e., where

chemically appropriate, in which A and B can change their locations. In view of the large plurality of the different claimed substances this understanding of the basic formula given above should be stressed in order to assure the intended scope and to conserve clarity and conciseness of the appended claims, concurrently.

Said substances are characterized by some specific range of amount of a dopant of one of or a combination of Chrome, Vanadium, or Manganese, or further transition metals.

In particular, any substance comprising components A_x, B_y, and oxygen O_z, in which substance said component A is a member of Alkaline metals (group IA in the periodic system of elements), or Alkaline Earth metals (group IIA), or Rare Earth elements, or Scandium, or Yttrium, and said component B is a transition metal being member of one of the groups IB to VIII, or a member of one of the groups IIIA, IVA, VA are substances which are able to solve the problem underlying to the present invention, when doped with a dopant of one of or a combination of transition metals, in particular but not exclusively with Chrome, Vanadium, or Manganese, the total dopant amount being larger than 0% and smaller than 5%, and preferably about 0,2% when $(BaSr)TiO_3$ is doped with Chrome only. Other preferred amounts of dopants are specific for each dopant element and substance used to be doped.

Having found the appropriate amount of dopant(s) a stable switching behavior required to operate a memory cell according to the invention can be provided.

Some additional specific requirements must be met by the combination of indices x,y,z in order to find the substances adapted to the inventional concepts. Each of the following items define a subclass of substances which show the desired switching

effect:

The combinations of indices x,y and z being defined by x= n+2, y= n+1, z= 3n+4, with 0 <= n reveal the so-called Ruddlesden Popper phases like e.g., Sr2RuO4 (xyz-index sequence 214) or Sr3Ru2O7 (xyz=327) and others.

The combinations of indices as defined above with n= 0 reveal a separate class of substances having a spinell structure as it is e.g., Mg2TiO4 (214), MgCr2O4, but the inverse arrangement, too, see e.g., Al2MgO4, Al2MnO4 where the B cations originally indexed by y are located on the position indexed by x and the A cations on the position indexed by y.

The combinations of indices x,y and z being defined by x= n+1, y= n+1, z= 3n + 5, with n= 1,2,3,4 reveal a separate class of substances which partly provide substances having an oxygen intercalation.

The combinations of indices x,y and z being defined by either of:
x= 1, y=1, z= 1,
and one of the indices x or y being 0, reveal exemplary substances like BeO,MgO, BaO, CaO,...NiO,MnO,CoO,CuO, ZnO, or

x= n, y= n, z= n+1 with n= 1 or 2
and one of the indices x or y being 0, for n=1, reveal substances like TiO2, VO2, MnO2, GeO2, CeO2, PrO2, SnO2,

for n=2, reveal substances likeAl2O3, CE2O3, Nd2O3, Ti2O3, Sc2O3, La2O3 or

x= n, y= n, z= 2n+1 with n= 2
and one of the indices x or y being 0, reveal exemplary substances like Nb2O5, Ta2O5 and others.

The combinations of indices x,y and z being defined by x= n, y= n, z= 3n, with n=1, or 2, or 3 reveal a separate class of substances for n= 1 the so-called perovskites, like $SrTiO_3$, $BaTiO_3$, $KNbO_3$, $LiNbO_3$, and others,

for n=2 Sr_2FeMoO_6 and similar substances are provided having a (226) index sequence.

The combinations of indices x,y and z being defined by x= n + 1, y= n, z= 4n + 1, with n= 1, or 2 reveal a separate class of substances.

For n= 1 substances having an index sequence (215) like Al_2TiO_5, Y_2MoO_5 and others are provided, and

$SrBi_2Ta_2O_9$ and similars are provided for n=2.

According to the concept of the present invention each of the classes mentioned above can be modified by varying the composition of the substance in order to achieve that at least one of said components A or B, respectively, is comprised of a combination of elements out of one group or out of several of the corresponding groups of A, and B, respectively.

A further modification is provided by providing a superlattice made by a combination of structural sub-units as it is published in 'E. Kaldis et al. (eds.), High-Tc Superconductivity 1996: Ten Years After Discovery, pp 95-108', having each a different n, and in which said sub-units are each a member of a corresponding homologous series obtained by oxygen intercalation. A further modification is provided by providing a superlattice made by a combination of sub-units of the Ruddlesden-Popper type structures having each a different n, and in which said sub-units are each a member of a corresponding homologous

series. In said lattice modifications lattice structures are formed in which single or multiple transition metal oxygen octahedra layers are separated by one or more block layers consisting of component A and oxygen.

One preferred member of that plurality of substances is $Ba_x Sr_{1-x}TiO_3$ with 0 <= x <= 0.7 and having a dopant of Chrome between 0 and 5%, preferably between 0 and 1%, even more preferably about 0,2%.

Others members of that plurality are materials according to $Ba_x Sr_{1-x}TiO_3$ with 0 <= x <= 0.7 and having a dopant of Vanadium between 0 and 5%.

Manganese is a preferred dopant, too, particularly in composition with chrome or vanadium.

Generally it should be noted that the dopant element(s) should be selected of course such that it (they) is (are) not yet contained in the components of the substance to be doped.

Further members of that plurality are perovskite related compounds with other transition metal cations such as Nb. Further dopants can be transition metal elements and combinations thereof, i.e., elements having their valence electron(s) on the d-orbital, i.e., 3d, 4d, or 5d -orbital.

When said material is used for example as a dielectric layer in a capacitor-like structure, it stays switched in either a high or a low conductivity state depending on a voltage pulse being applied to it until it is switched into the other state by applying a new voltage pulse. Thus, said capacitor-like structure having such a complex dielectric material has a resistance which can be varied by applying short voltage or,

alternatively, short current pulses to the embedding electrodes.

As the most decisive electrical property of said element is the change in resistance depending on a defined, applied voltage pulse between the two terminals of the element said capacitor-like structure can be regarded as a 'switchable resistor'. Said switching behavior is skown to be effectuated by a voltage or current driven hystersis behavior.

Due to said property it is possible to store digital information by different values of resistance, i.e., by associating a high resistance state with a logic '0' and a low resistance state with a logic '1'. The actual state and thus the stored information can be read out by measuring the leakage current as it is relatively large with low resistance of the dielectric layer and vice versa. Thus, the leakage current which impedes the performance of prior art DRAM technology can be usefully taken for reading the stored value. According to the invention neither the static charge of a capacitor nor the polarization of any ferroelectric material is needed to be used for storing information but, instead, its resistance.

Thus, a new way to store information is followed by realizing the above mentioned inventional concepts.

The material according to the present invention with the characteristics of one of claims 1 to 21 when used for e.g. RAM cells has the advantage, in relation to prior art memory cells that new cells can be constructed just comprising a single capacitor-like structure device with only one pair of electrode terminals for operating it, i.e. to read from, to write into or to erase without a transistor arrangement being necessarily coupled with a capacitor used in prior art to perform the operating functions of a prior art DRAM cell. One terminal of

the new cell is connected to ground and the other is used for writing, erasing or just reading.

Thus, RAM cells can be constructed to use considerably less space on a chip and considerable less manufactoring steps.

Further, the inventional material has a remarkable high retention time of at least several days to several weeks and can thus be used as a non-volatile memory. Thus a double advantage can be achieved: first, the full time is available for the read and write processes because the refresh cycles and therefor the refresh circuitry are not required anymore and, secondly, a data storage security is increased as a loss of power supply does not imply a loss of stored data.

Basically, the inventional memory cell can be operated in either a voltage controlled or in a current controlled regime, i.e. information can be stored by applying voltage pulses or by applying current pulses. In both cases the information is read by measuring the leakage current. For purposes of improved clarity of the inventional disclosure, however, only the voltage regime is described in the detailed description down below.

Finally, for example in the voltage controlled regime the current flowing when reading a '1' compared to that one when reading a '0' value is about 20 times larger due to the difference in resistance. This feature can advantageously be used for storing more than only one bit in the same cell. Thus, a plurality of two, three, or more bits can be stored or removed by applying different voltage pulses, single pulses or sequences thereof having different shape, level, or duration or being different in number to write and erase. A sufficiently large distance between the different levels can hereby be maintained.

3. BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and is not limited by the shape of the figures of the accompanying drawings in which:

Fig. 1 is a schematic drawing of a perovskite oxide capacitor-like structure usable as a memory cell according to the invention,

Fig. 2 shows current-voltage characteristics of a 300 nm thick Cr doped oxide capacitor-like structure according to the invention,

Fig. 3a to 3c show the principles of operation of the capacitor-like structure analyzed in fig. 2 as a memory device, and

Fig. 4 shows a schematic circuit diagram representing the arrangement of a 4-Bit-memory cell according to the invention.

4. DESCRIPTION OF THE PREFERRED EMBODIMENT

With general reference to the figures and with special reference now to fig. 1 the essential structure of a memory cell comprising a capacitor-like structure according to the invention is described in more detail.

A thin film capacitor-like structure 10 comprising an oxide base electrode 12 made from $SrRuO_3$ and an oxide insulator layer 14 made from $(BaSr)TiO_3$ slightly doped with chrome (Cr) for the insulating material and a metallic (Au) top electrode 16 on a $SrTiO_3$ substrate 18 was fabricated with pulsed laser deposition.

One terminal 20 is connected to said top electrode 16, the other terminal 22 is connected to said base electrode 12.

In an experimental arrangement setup for testing the basic switching behavior and further physical properties of the inventional memory cell the insulator layer 14 thickness was 300 nanometers.

Said insulator layer 14 was doped with chrome (Cr) at an amount of 0,2%.

The leakage current was measured as it is depicted in the drawing as a function of the bias voltage generated by a DC voltage source 24 between said terminals 20,22.

With respect to fig. 2a to 2c the leakage current voltage characteristic is illustrated in fig. 2a linearly, in fig. 2b with a logarithmic leakage current scale of its absolute amount and in fig. 2c with both logarithmic scales.

For small applied bias voltages like several 10 mV a linear current voltage characteristic (IVC) can be observed. A quadratic dependence of the current from the applied voltage can be seen for moderate applied voltages as several 100 mV.

This IVC shape and behavior can be described as space charge limited current. Larger applied voltages result in an exponential like rise of the leakage current with increasing applied voltages.

The capacitor-like structure 10 according to the present invention shows a reproducible switching behavior causing a hysteresis loop in the current voltage characteristic, described next below:

A large negative bias voltage -negative with respect to the $SrRuO_3$ electrode- leads to a sudden increase of the leakage current, depicted at about -0,8 Volt. Sweeping back to large positive bias voltage the leakage current drops back to a low value again depicted at + 0,7 Volt. Said sudden increase and said sudden drop back of leakage current are the essential features of the detected switching phenomenon.

According to the invention it is possible to operate the capacitor-like structure 10 as a very simple memory device, i.e memory cell in a RAM due to and with the described underlying switching behavior. This will be illustrated in conjunction with figs 3a to 3c.

Basically, by applying a negative voltage pulse to the capacitor-like structure the system is switched into a low resistance state which can be regarded as storing information. A positive pulse recovers the high resistance state of the device and the information is removed, i.e., erased.

As can be seen in fig. 3a a series of 300ms long voltage pulses depicted as sharp peaks were applied to the capacitor-like structure. The negative pulses are used to write information which after a certain delay is removed by a positive pulse. Between the pulses a small negative voltage is switched on and off periodically to read the information and to simulate a realistic readout process. 120 reading cycles each having a duration of 1 sec are performed after each write or erase pulse. This readout procedure is schematically depicted in a better time resolution by the zoomed portion in fig. 3a.

The readout from the device 10 is performed by measuring the leakage current flowing at a small applied voltage of 0.2 V as it is depicted in fig. 3b which shows current spikes occurring during write and erase followed by the readout period with currents one order of magnitude lower. Fig. 3c is a leakage current scale enlargement of fig. 3b and clearly shows the low and high resistance states of the device 10 obtained by writing and erasing the information.

Two different resistance states can be clearly separated: The upper state around 30 nano Amperes yielding a resistance of R=6,6 Mega Ohm and the bottom part state having a leakage current of 650 nano Amperes yielding a resistance of R=300 kilo Ohm. The upper state will now be associated with a logic state '0' and the bottom state with a logic state '1'.

The '1' resistance value is 20 times smaller than the '0' value. A clear separation of the two logic states is thus achieved.

Additionally, this remarkable dependence of the resistance on the applied voltage pulse together with the hysteresis behavior allows to write different values to the memory cell and to read

them out with a single pre-specified read-out voltage. This so-called multi-level switching phenomenon is discussed later in more detail.

During the experimental measuring runs in this example information was written and erased during 300ms - the duration of the sharp peaks - and stored for 240s. The time to store and erase information was a specifically selected experimental parameter but is not limited by the memory device itself. Therefore, the ultimate speed for the write/erase process is much higher.

The time over which information can be stored is much larger than those 240s measured experimentally.

If one analyzes the switching behavior of such capacitor-like structures with varying Cr doping it can be observed up to now that the switching behavior is more pronounced for slightly Cr doped structures, i.e. the best results are obtained with Cr-doping around 0,2%. For these capacitor-like structures the difference between "0" and "1" was the best with adequate reproducibility.

Summarizing the main aspects of the inventional concepts capacitor-like structures having a DC-resistance changing sensitively with the applied voltage pulse and consisting of oxides doped according to the invention can be operated as a memory device with the following intriguing properties:

First they have a very simple structure because the whole memory cell is a capacitor-like structure. Thus they can be operated with only two terminals with a single terminal for read, write and erase. Thus, they are best adapted for ULSI technology.

Further, the difference in resistance between the '0' value and '1' value is at least one order of magnitude as can be seen from fig. 3c. As can be seen further from the IVC depicted in fig. 2a, a large resistance range can thus be exploited to store a plurality of different logical values, i.e., the so-called multi-level switching can be achieved. Herefore, a plurality of write pulses different in size, etc, as mentioned earlier can be applied to write specific logical values into the memory cell, in order to realize not a dual system but, e.g., a digital decimal system based on 10 different logical values being able to be written into and to be read from said memory cell in subsequent write /read /erase cycles.

Finally, the information is stored over long times which is a remarkable advantage compared to conventional DRAM cells.

With reference to fig. 4 a schematic circuit diagram representing the arrangement of a 4-Bit-memory cell according to the invention is shown.

Four of the inventional memory cells are arranged linearly in order to represent a 4 bit memory circuit addressed via an address line 28 by a decoder 30 the outputs of which are connected to a respective top electrode 16. The base electrodes 22 thereof are each connected to ground. A write, erase, or read voltage pulse can be applied to a selected memory cell 10 through the bias line 32. The different memory cells output current is evaluated through the output line 34.

In a similar way a matrix like arrangement can be achieved by connecting the base electrodes of a row of the memory cells with a further decoder.

It is obvious that the arrangement of the particular components 12, 14, 16, 18 of the inventional capacitor-like structure on a chip will be adapted to the requirements imposed by the specific integration level which is intended to be achieved with the chip. A broad spectrum of different architectures can thus be realized which are all comprised by the inventional concept.

Beside the capability of the device 10 described above to store information it is possible to use a system comprising an inventionally doped capacitor-like structure 10 as an active switching element in electric or electronic circuits.

In this area of interest a switching operation is not restricted to a specific resistance value. Devices having a resistance of some Mega Ohm can be operated at a voltage between 1 Volt and 5 Volt for writing and erasing and at a voltage between 0,05 Volt and 0,5 Volt for reading. Devices having a smaller resistance can also be operated, however at different voltages.

Further, the inventional concept provides for an application of the inventional substance for constructing EEPROMs, logic gates as e.g. AND gates, OR-gates, tunable capacitors and further complex logic circuits.

Particularly, when silicon (Si) or other semiconductor substrates are taken as substrate material instead of strontium titanate the current prior art semiconductor materials can be grown on the substrate thus providing the ability to join conventional semiconductor technology with the memory cells or switching elements, respectively, of the inventional concepts.

In the foregoing specification the invention has been described with reference to a specific exemplary embodiment thereof. It will, however, be evident that various modifications

particularly relative to the application of a large variety of different substances as they are claimed in the appended claims may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims.

The specification and drawings are accordingly to be regarded as illustrative rather than in a restrictive sense.

In particular the thickness of the insulator layer as well as the lateral dimensions of the cell and the applied bias voltages or bias currents, respectively, can be varied as it is required by any specific purpose imposed by any of a plurality of varying chip designs.

Also the material selection for the bottom electrode can be varied as well. A simple metal like platinum (Pt) is suited as well.

Also for the top electrode the material can be varied as well. Au, Pt are suited materials, but principally, all metals and conducting oxides are suited materials for both, top and bottom electrodes.

5. LIST OF REFERENCE SIGNS

10	capacitor-like structure arrangement
12	base electrode
14	insulator layer, dielectric
16	top electrode
18	substrate
20, 22	terminals
24	DC voltage source
28	address line
30	decoder
32	bias line
34	output line

6. CLAIMS

1. A substance comprising components A_x, B_y, and oxygen O_z, in which substance

   said component A is a member of Alkaline metals (group IA), or Alkaline Earth metals (group IIA), or Rare Earth elements, or Scandium, or Yttrium,

   said component B is a transition metal being member of one of the groups IB to VIII, or a member of one of the groups IIIA, IVA, VA,

   the combinations of indices x,y and z being defined by $x= n+2$, $y= n+1$, $z= 3n+4$, with $0 <= n$,

   said substance being characterized by a dopant of one of or a combination of different transition metals, the total dopant amount being larger than 0% and smaller than 5%.

2. The substance according to the preceding claim, comprising a dopant of Chrome or Vanadium at an amount greater than 0% and smaller than 5%, preferably about 0,2%.

3. The substance according to the preceding claims, in which at least one of said components A or B, respectively, is comprised of a combination of elements out of one group or out of several of the corresponding groups of A, and B, respectively.

4. The substance according to one of the preceding claims, comprising a superlattice made by a combination of structural sub-units having each a different n, said sub-units being each a member of a corresponding homologous series.

5. A substance comprising components A_x, B_y, and oxygen O_z, in which substance

said component A is a member of Alkaline metals (group IA), or Alkaline Earth metals (group IIA), or Rare Earth elements, or Scandium, or Yttrium,

said component B is a transition metal being member of one of the groups IB to VIII, or a member of one of the groups IIIA, IVA, VA,

the combinations of indices x,y and z being defined by $x= n+1$, $y= n+1$, $z= 3n+5$, with $n= 1,2,3,4$,

said substance being characterized by a dopant of one of or a combination of different transition metals, the total dopant amount being larger than 0% and smaller than 5%.

6. The substance according to the preceding claim, comprising a dopant of Chrome or Vanadium at an amount greater than 0% and smaller than 5%, preferably about 0,2%.

7. The substance according to the preceding claims 5 or 6, in which at least one of said components A or B, respectively is comprised of a combination of elements out of one group or out of several of the corresponding groups of A, and B, respectively.

8. The substance according to one of the preceding claims 5 to 7, comprising a super lattice made by a combination of structural sub-units having each a different n, said sub-units being each a member of a corresponding homologous series.

9. A substance comprising components A_x, B_y, and oxygen O_z, in which substance

said component A is a member of Alkaline metals (group IA), or Alkaline Earth metals (group IIA), or Rare Earth elements, or Scandium, or Yttrium,

said component B is a transition metal being member of one of the groups IB to VIII, or a member of one of the groups IIIA, IVA, VA,

the combinations of indices x,y and z being defined by either of:
$x= 1$, $y=1$, $z= 1$,
and one of the indices x or y being 0, or

$x= n$, $y= n$, $z= n+1$ with $n= 1$ or 2
and one of the indices x or y being 0, or

$x= n$, $y= n$, $z= 2n+1$ with $n= 2$
and one of the indices x or y being 0,

said substance being characterized by a dopant of one of or a combination of different transition metals, the total dopant amount being larger than 0% and smaller than 5%.

10. The substance according to the preceding claim, comprising a dopant of Chrome or Vanadium at an amount greater than 0% and smaller than 5%, preferably about 0,2%.

11. The substance according to the preceding claims 9 or 10, in which one of said components A or B, respectively, is comprised of a combination of elements out of one group or out of several of the corresponding groups of A, and B, respectively.

12. The substance according to one of the preceding claims 9 to 11, comprising a superlattice made by a combination of structural sub-units.

13. A substance comprising components A_x, B_y, and oxygen O_z, in which substance

said component A is a member of Alkaline metals (group IA), or Alkaline Earth metals (group IIA), or Rare Earth metals, or Scandium, or Yttrium,
said component B is a transition metal being member of one of the groups IB to VIII, or a member of one of the groups IIIA, IVA, VA,
the combinations of indices x,y being defined by
$x= n$, $y= n$, $z= 3n$ with $n=1$, or 2, or 3

said substance being characterized by a dopant of one of or a combination of different transition metals, the total dopant amount being larger than 0% and smaller than 5%.

14. The substance according to the preceding claim, comprising a dopant of Chrome or Vanadium at an amount greater than 0% and smaller than 5%, preferably about 0,2%.

15. The substance according to the preceding claims 13 or 14, in which n equals 1.

16. The substance according to the preceding claims 13 to 15, in which at least one of said components A or B, respectively, is comprised of a combination of elements out of one group or out of several of the corresponding groups of A, and B, respectively.

17. The substance according to one of the preceding claims 13 to 16, comprising a superlattice made by a combination of structural sub-units having each a different n.

18. A substance comprising components A_x, B_y, and oxygen O_z, in which substance

said component A is a member of Alkaline metals (group IA), or Alkaline Earth metals (group IIA), or Rare Earth elements, or Scandium, or Yttrium,

said component B is a transition metal being member of one of the groups IB to VIII, or a member of one of the groups IIIA, IVA, VA,

the combinations of indices x,y being defined by
$x= n + 1$, $y= n$, $z= 4n + 1$ with $n = 1$, or 2

said substance being characterized by a dopant of one of or a combination of different transition metals, the total dopant amount being larger than 0% and smaller than 5%.

19. The substance according to the preceding claim, comprising a dopant of Chrome or Vanadium at an amount greater than 0% and smaller than 5%, preferably about 0,2%.

20. The substance according to the preceding claims 18 or 19, in which at least one of said components A or B, respectively, is comprised of a combination of elements out of one group or out of several of the corresponding groups of A, and B, respectively.

21. The substance according to one of the preceding claims 18 to 20, comprising a superlattice made by a combination of structural sub-units having each a different n, said sub-units being each a member of a corresponding homologous series.

22. Use of the substance according to one of the preceding claims for making regions having a switchable resistance in microelectronic devices in a semiconductor chip.

23. Use of the substance according to one of the preceding claims 1 to 21 for producing a capacitor-like structure having a high ohmic dielectric as an electric circuit element.

24. Semiconductor chip comprising a substance according to one of the preceding claims 1 to 21.

25. Chip according to the preceding claim characterized by comprising memory cells having at least one region consisting of the substance according to one of the claims 1 to 21.

26. Chip according to the preceding claim characterized by comprising memory cells each comprising at least one capacitor-like structure comprising a region being subjectable to a controllable resistance change and being made of the substance according to one of the preceding claims 1 to 21.

27. Memory cell arrangement comprising a substance according to one of the preceding claims 1 to 21.

28. Electronic switching device comprising a region being subjectable to a controllable resistance change and being made of the substance according to one of the claims 1 to 21.

29. Electronic circuit comprising a device according to the preceding claim.

30. A method to operate a memory cell arrangement according to claim 27 comprising the steps of:

applying a predetermined pulse of write bias voltage to said cell arrangement for writing a data into it,

applying a read voltage to said cell arrangement smaller in size than said write bias voltage pulse,

associating with said data a value of current flowing through said cell arrangement resulting from and individual for said write voltage pulse applied before.

31. The method according to the preceding claim, further comprising the step of:

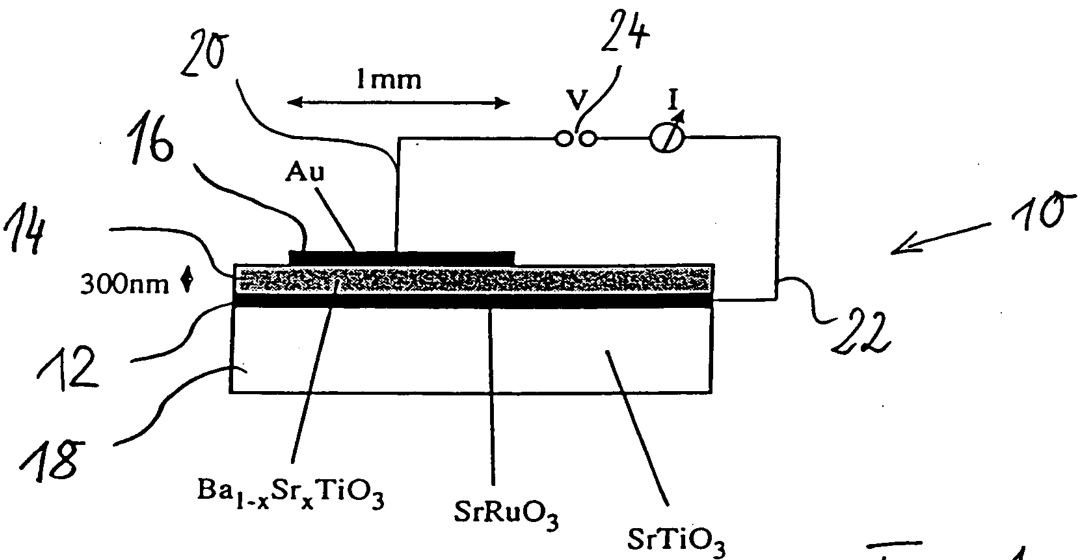
applying a predetermined pulse of erase bias voltage to said cell arrangement for erasing a data from it.

7. SUMMARY

The basic discovery underlying the present invention concerns a plurality of oxide substances, i.e., materials for use in microelectronic and in electronic circuits and particularly for use in semiconductor chips which combines both, a switching phenomenon in resistance and a built-in memory.

One preferred member of that plurality is $Ba_x\ Sr_{1-x}TiO_3$ with 0 <= x <= 0.7 and having a dopant of Chrome between 0 and 5%, preferably between 0 and 1%, even more preferably about 0,2%.

When said substance is used for example as a dielectric layer in a capacitor-like structure it stays switched in either a high or a low conductivity state depending on the voltage pulse being applied to it until it is switched into the other state by applying a new voltage pulse. Thus it is possible to store digital information by different values of resistance, i.e., by associating a high resistance state with a logic '0' and a low resistance state with a logic '1'. The actual state and thus the stored information can be read out by measuring the leakage current as it is relatively large with low resistance of the dielectric layer and vice versa. Even multi-level switching is able to be realized. ~~(fig. 2a)~~ [4]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20
1mm
V
I
16
Au
10
14
300nm
22
12
18
$Ba_{1-x}Sr_xTiO_3$
$SrRuO_3$
$SrTiO_3$

Fig. 1

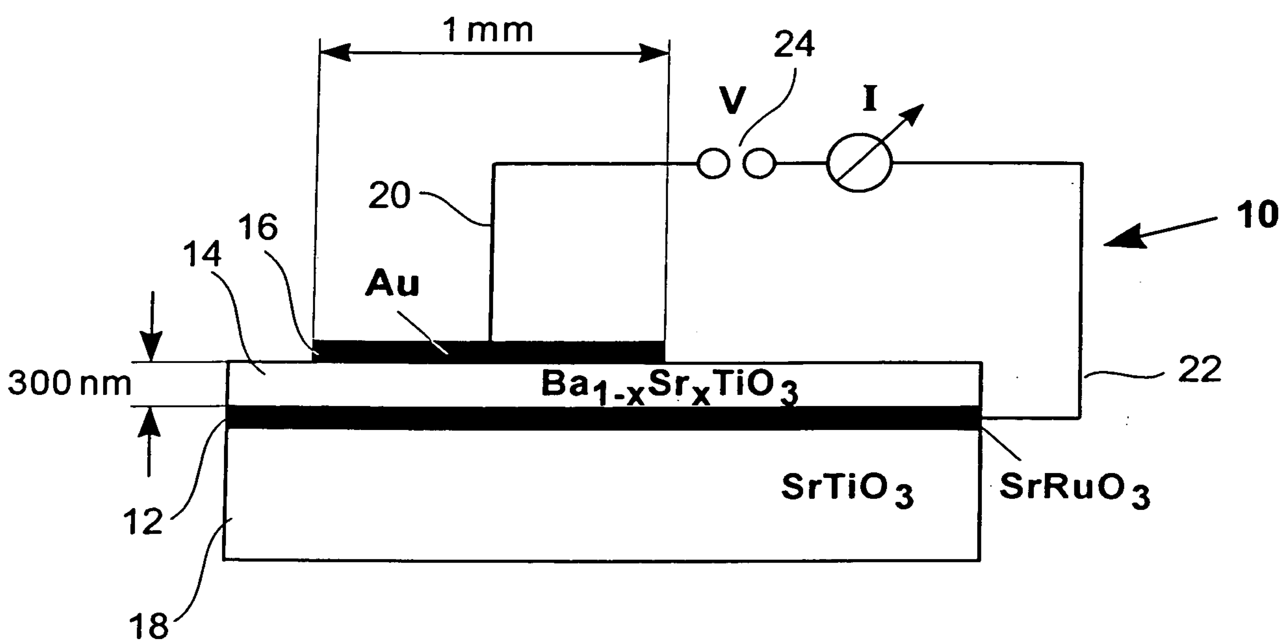

1 mm
24
V
I
20
10
16
14
Au
300 nm
$Ba_{1-x}Sr_xTiO_3$
22
12
$SrTiO_3$
$SrRuO_3$
18

Fig. 1

SZ 9-98-049

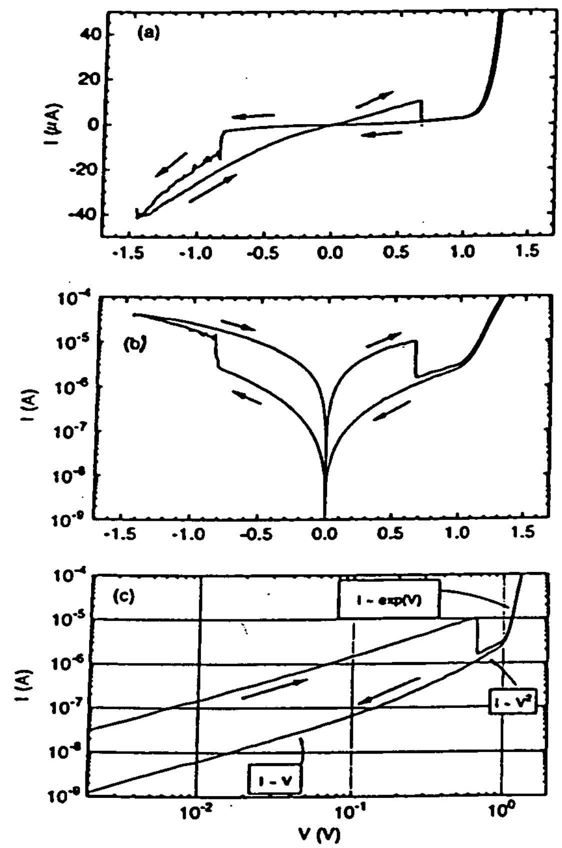
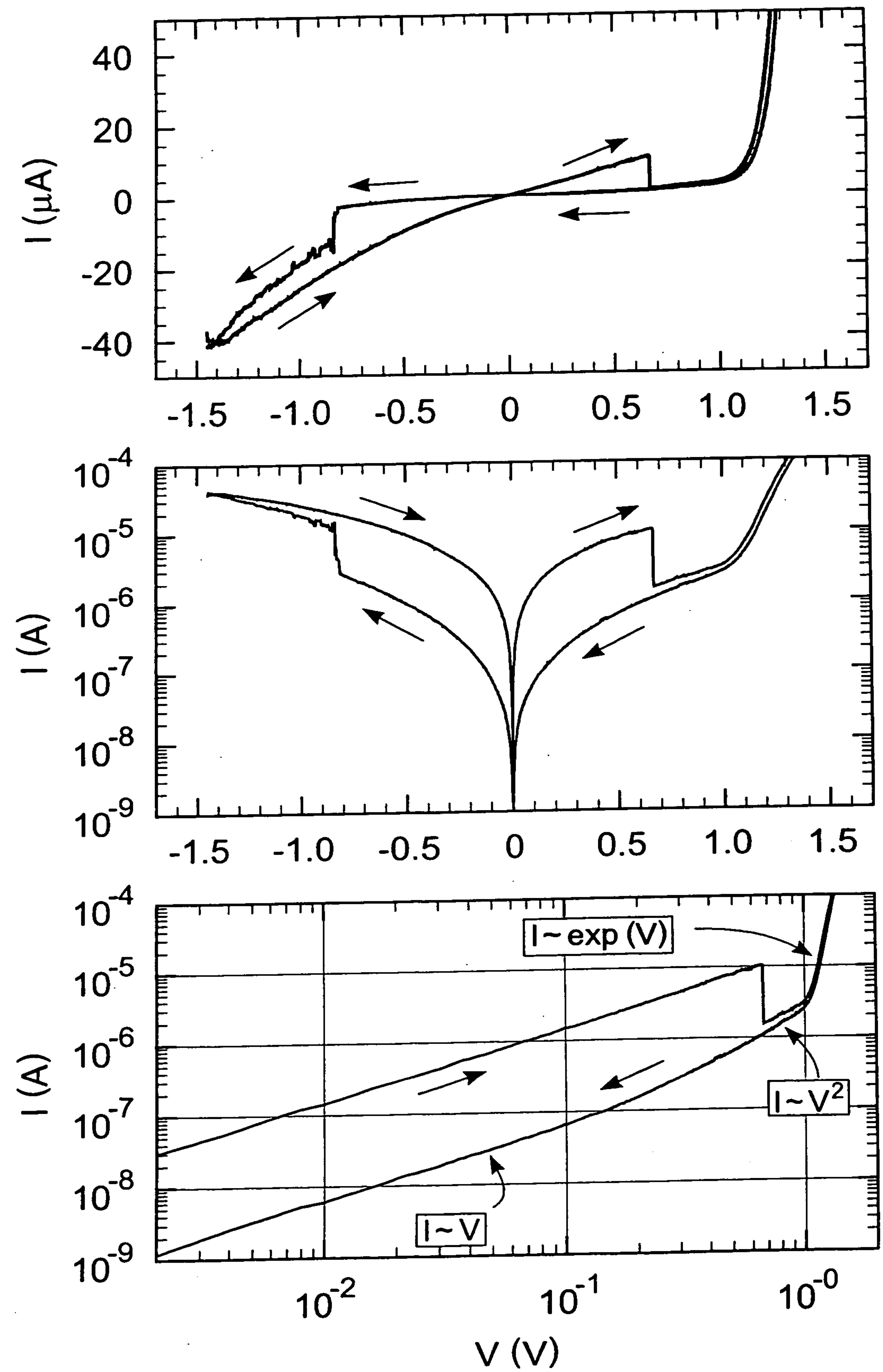


Fig. 2

Fig. 2a

Fig. 2b

Fig. 2c



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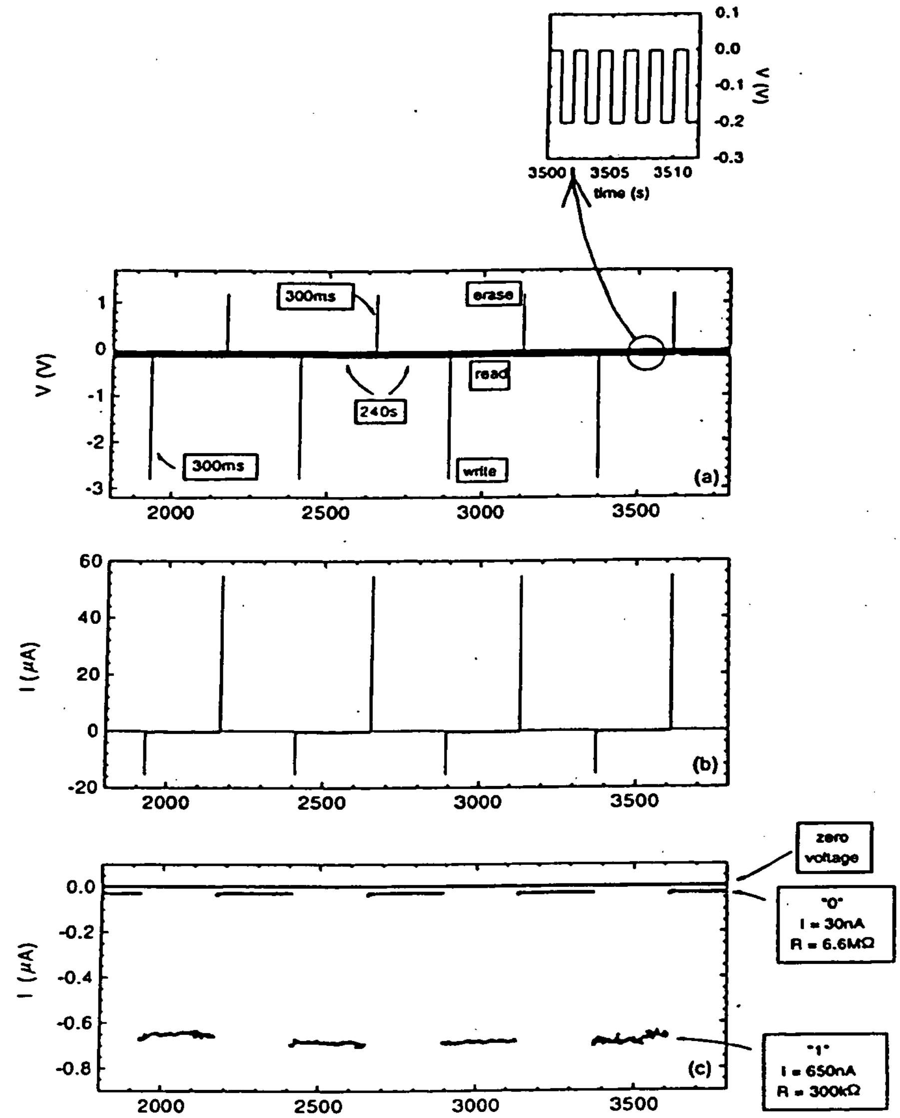
0.1
0.0
-0.1
-0.2
-0.3
V (V)
3500
3505
3510
time (s)
300ms
erase
read
240s
300ms
write
(a)
V (V)
1
0
-1
-2
-3
2000
2500
3000
3500
60
40
20
0
-20
I (μA)
(b)
0.0
-0.2
-0.4
-0.6
-0.8
I (μA)
(c)
zero voltage
"0"
I = 30nA
R = 6.6MΩ
"1"
I = 650nA
R = 300kΩ

Fig.3

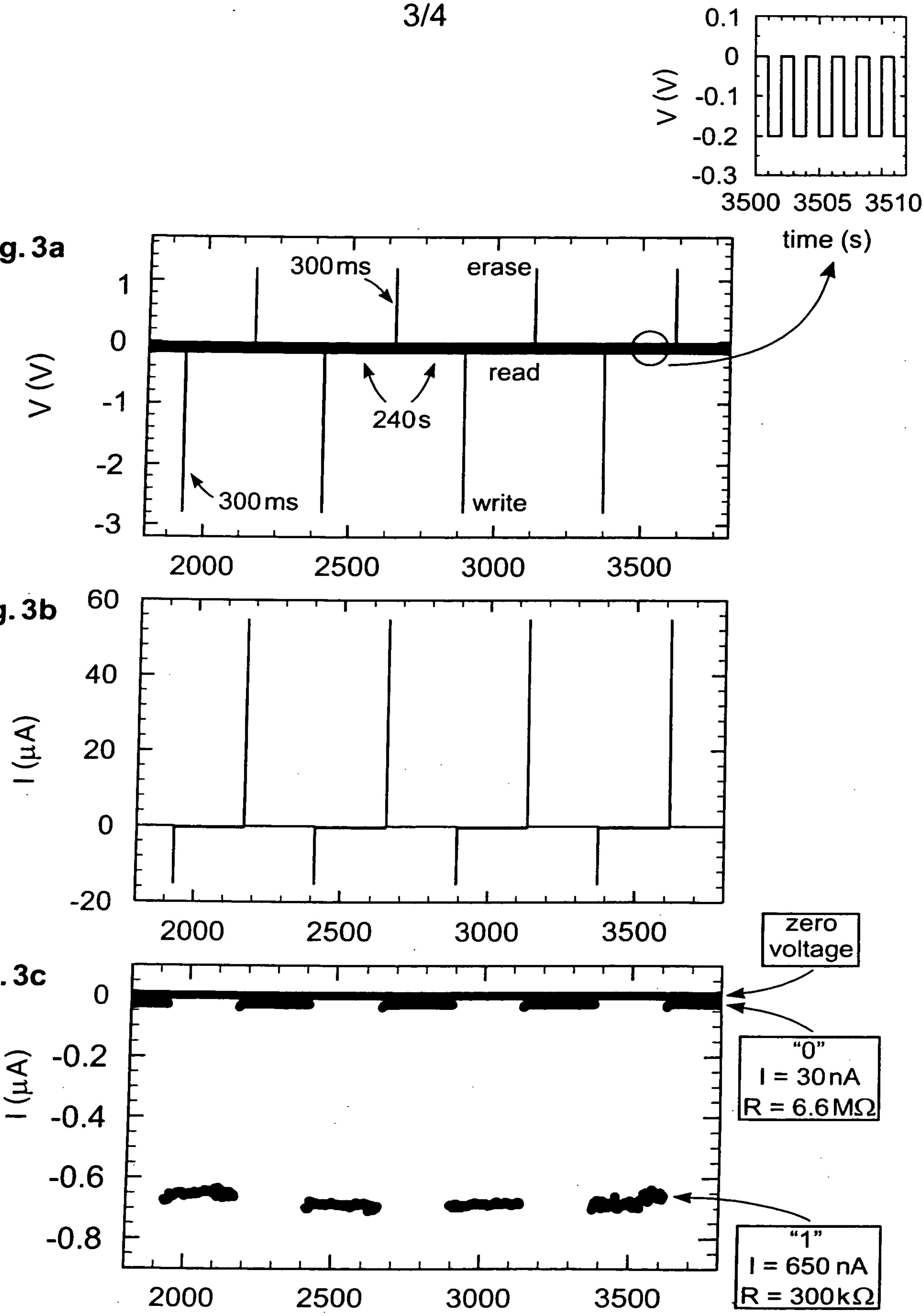

Fig. 3a

Fig. 3b

Fig. 3c

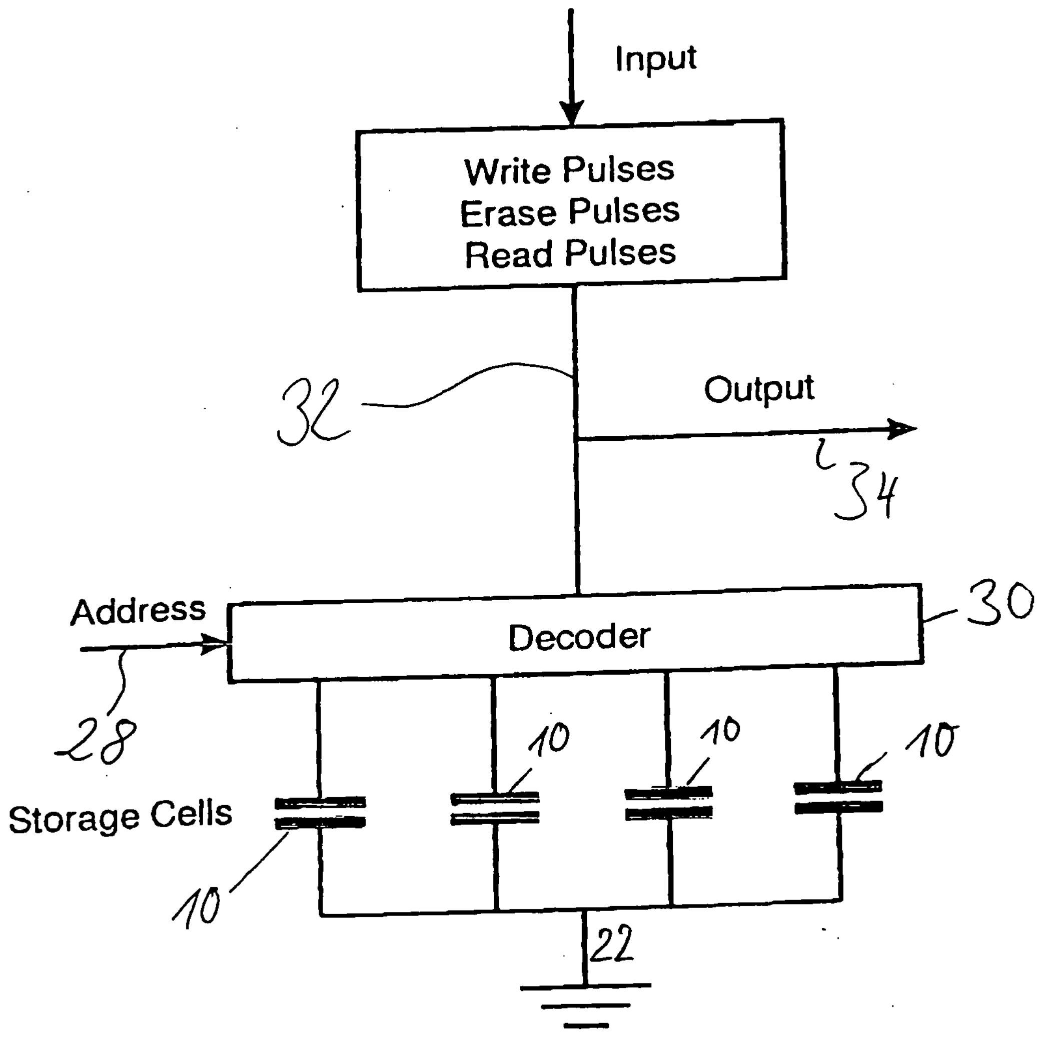
Input
Write Pulses
Erase Pulses
Read Pulses
32
Output
34
Address
Decoder
30
28
10
10
10
Storage Cells
10
22

Fig. 4

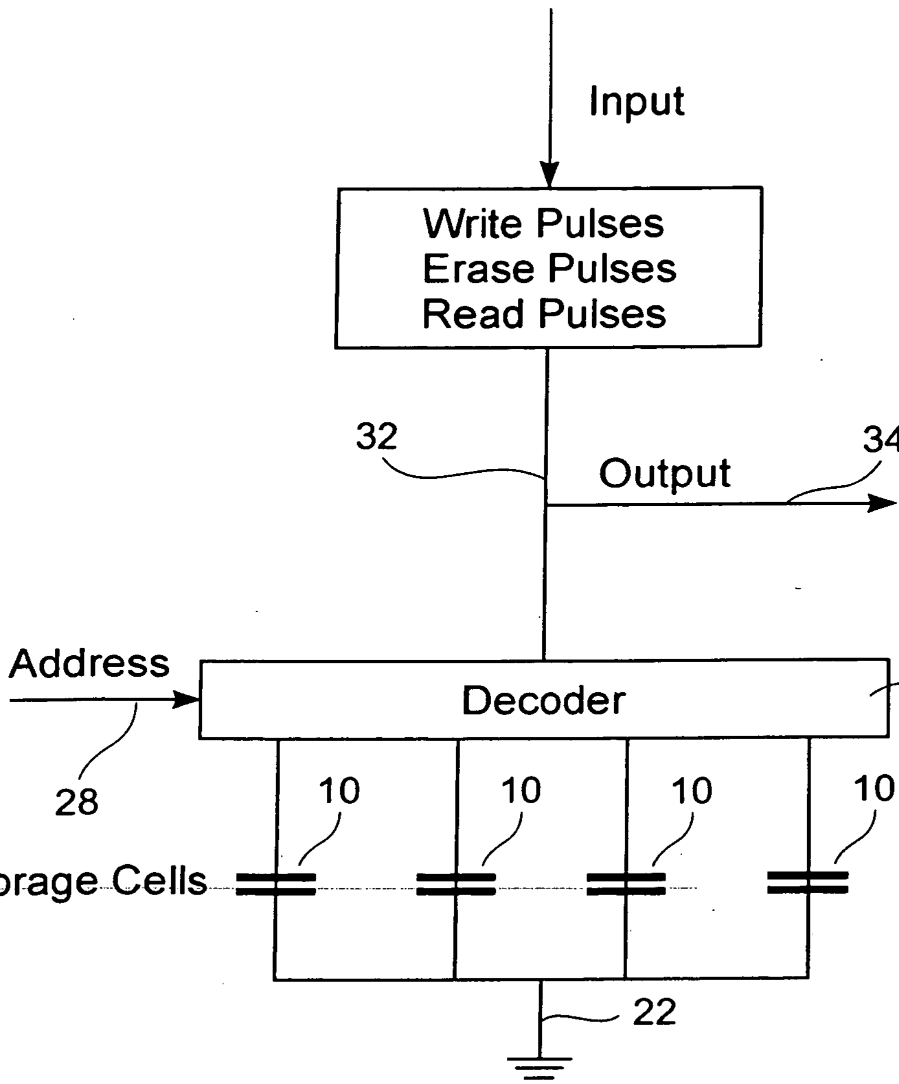
Input
Write Pulses
Erase Pulses
Read Pulses
32
Output
34
30
Address
Decoder
28
10
10
10
10
Storage Cells
22

Fig. 4